Latest developments of MCP detectors at Berkeley

*Oswald Siegmund, Jason McPhate, Anton Tremsin and John Vallerga**

Space Sciences Laboratory
U. California, Berkeley

*** jvv@ssl.berkeley.edu**

Microchannel Plate Detectors
Where are they?

Recent MCP systems in Space based Astrophysics and Planetary Missions:

HST-COS, GALEX, LITES, JUNO, LRO-LAMP, Rosetta-ALICE, Pluto-ALICE, CHESS, FORTIS, SISTINE, ICON, GOLD, EMM-EMUS, SSULI, Solar Orbiter, SPICE, JUICE-UVS, INFUSE.

In progress:

SPRITE, MOBIUS, MANTIS, ASPERA, EUROPA-UVS, EUVST.

Proposals:

Cubesats, Rockets, MIDEX, PROBE.

Plus:

Neutron/X-ray beam lines, High Energy Physics, Synchroton light sources

Microchannel Plate Detectors
How they work

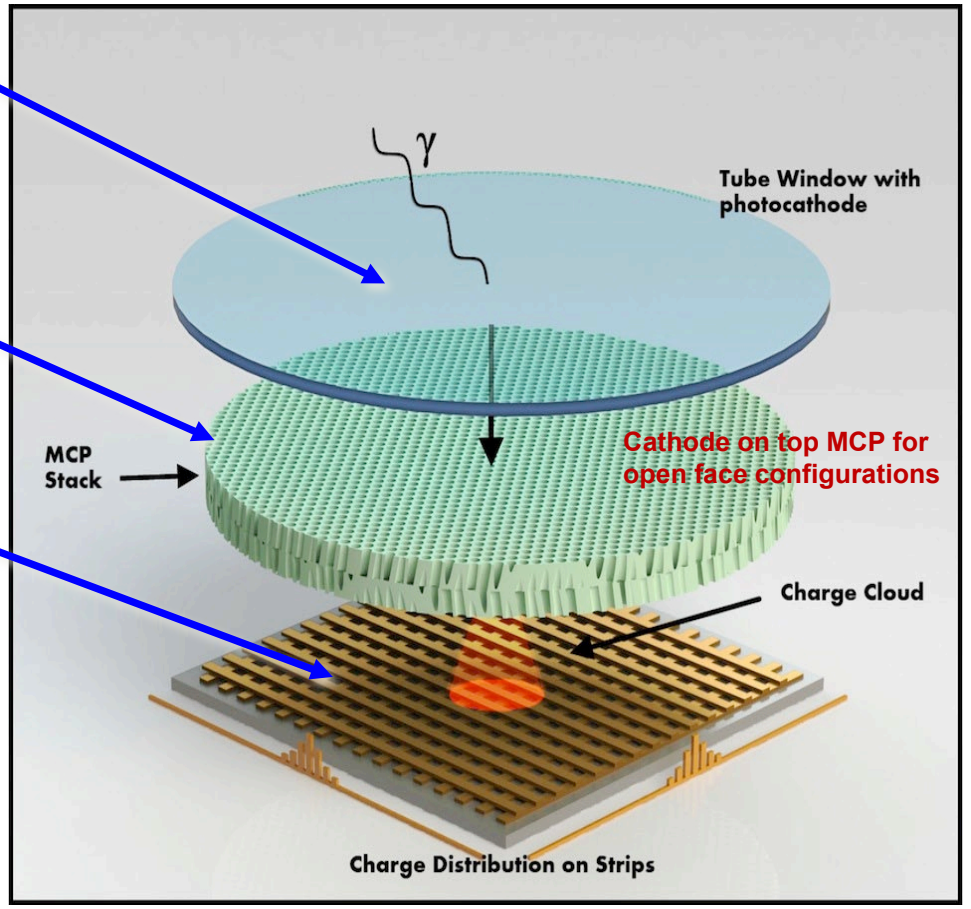
Photocathode converts photon to electron

Alkali halides, Multialkali, GaAs, GaN

MCP(s) amplify electron by 10^4 to 10^7

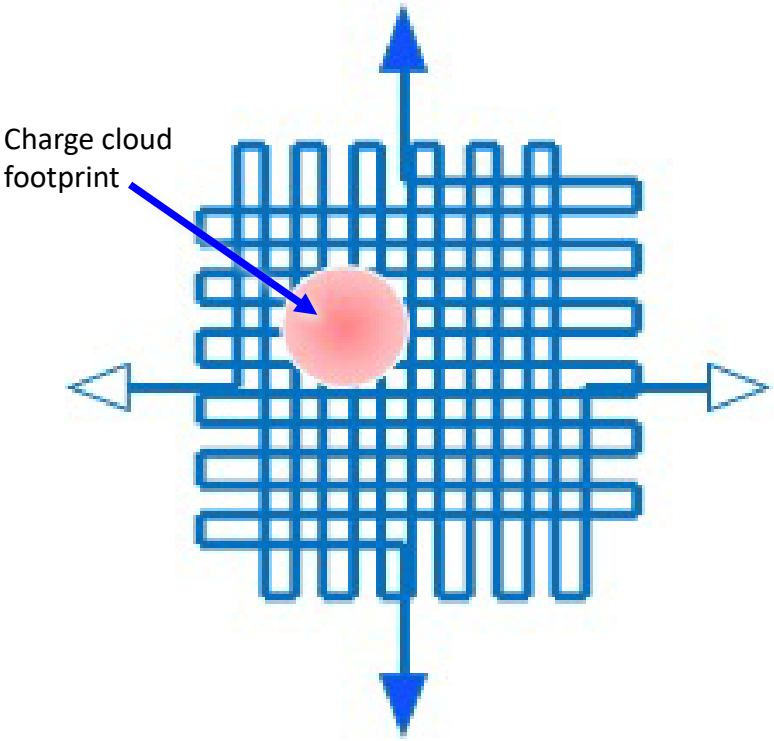
Patterned anode measures charge centroid

Cross strip, Cross delay line, Timepix ASIC or Phosphor.



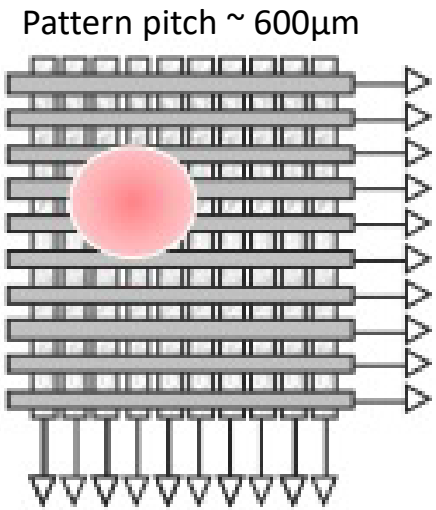
Developments underway: Atomic layer deposited MCPs, large area borosilicate MCP substrates, cross strip and Timepix4 readouts, large area sealed tubes, and ASIC processing electronics

MCP readout anode types (partial list)



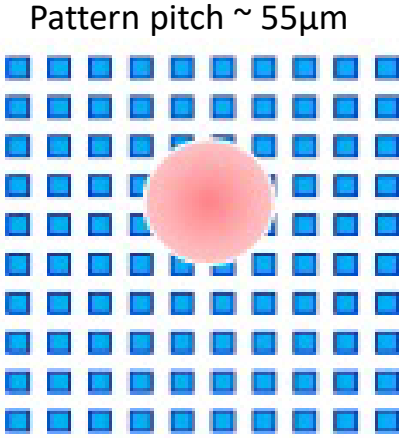
Cross Delayline (XDL)

4 amplifiers
Gain ~ 10^7
Rate ~ 200kHz



Cross Strip (XS)

2 x N amplifiers
Gain ~ 10^6
Rate ~ 20MHz



Timepix4 ASIC

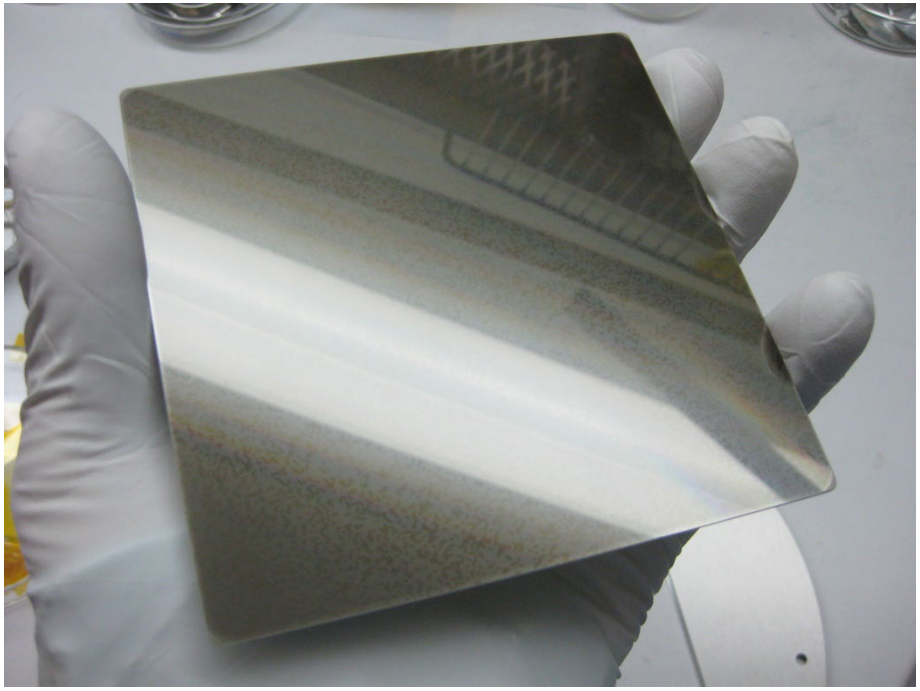
512 x 448 amplifiers
Gain ~ 50,000
Rate ~ 200MHz per chip

Large Area 10µm pore ALD MCPs

We are using 108mm ALD MCPs with 10µm pores for 5cm & 10cm XS tubes --- Incom has made 10µm pore MCPs as large as 20cm.

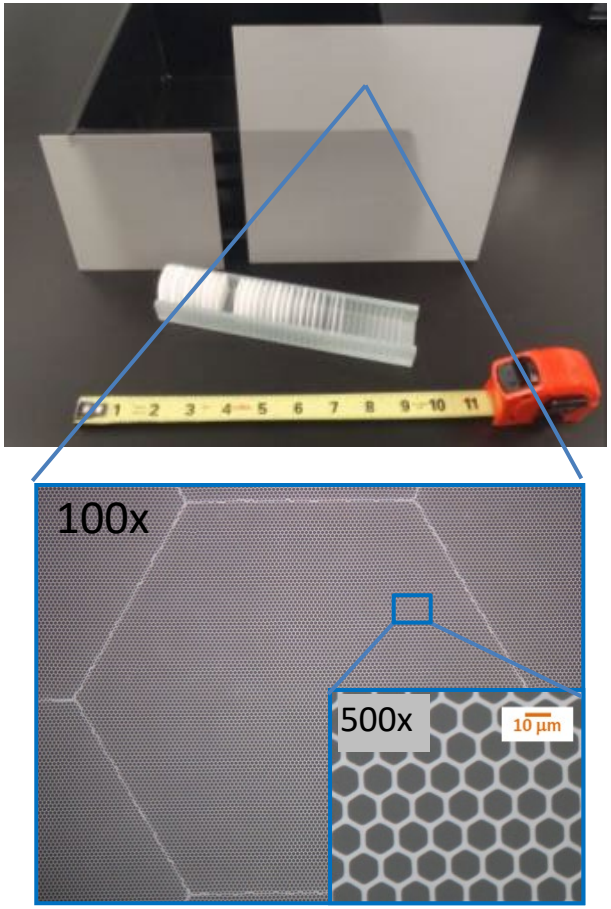
Borosilicate micro-capillary arrays (Incom, Inc.). Fabricated using hollow tubes (6 µm, 10 µm, or 20 µm pores, 13° bias, l/d typically 60:1, open area ~73%) without etching. Separate resistive and secondary emissive layers are applied (ANL, Incom) using atomic layer deposition to function as MCPs.

Large Areas, --- --20 × 20 cm^2 - 20 µm & 10 µm pores.
Long Device Lifetimes, -- Stable gain to >4 x 10^{13} events cm^{-2}
Low γ-Ray Efficiency, -- <0.7% vs 2% (standard MCP) for MeV γ events
Radiation hard, -->100 kRad at nuclear reactor - no long term effects.
Low Background, -- <0.05 events sec^{-1} cm^{-2}, (<2 events $pixel^{-1}$ $fortnight^{-1}$)



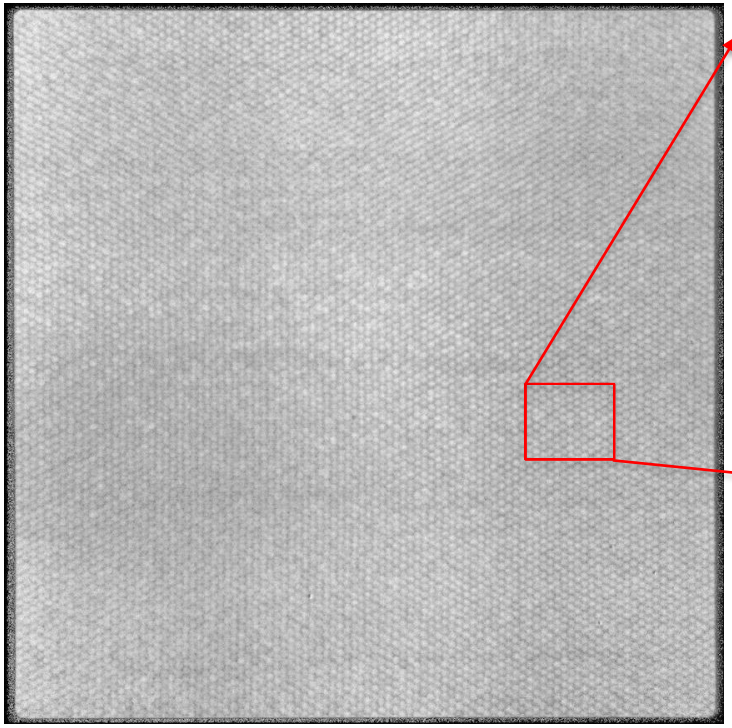
108mm format 10µm pore ALD-borosilicate substrate MCP.

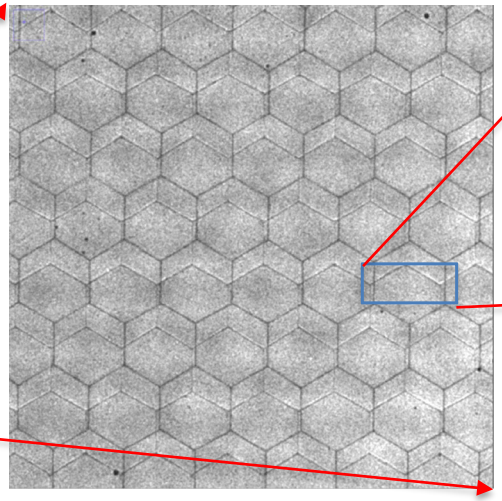
203mm 10µm pore MCPs made. Borosilicate MCPs are very flat, stable compared to conventional MCPs. 20µm 208mm MCPs shaken >15 x, flown 4x with no failures (DEUCE, CU).

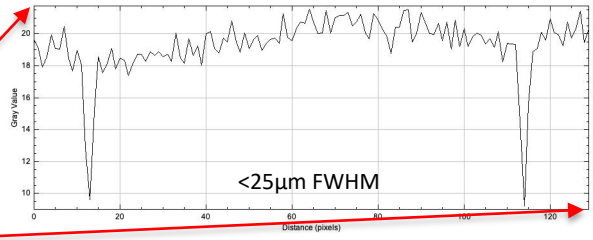


ALD 10µm Pore MCP Tests – XS Imaging

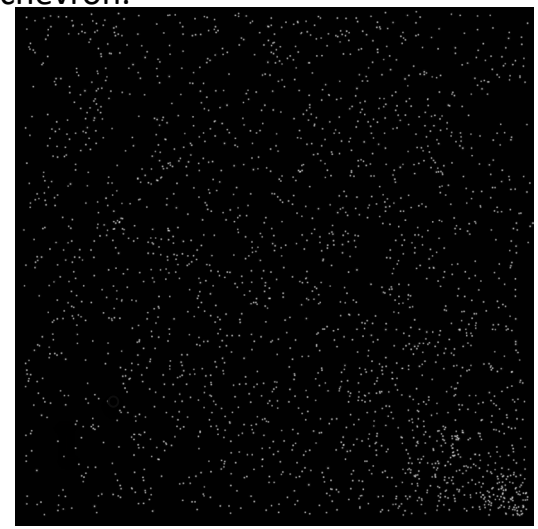
108 x 108mm Incom 10 µm pore, 13° bias, 70% OAR, L/D 60:1, MgO ALD chevron.
+ CsI cathode



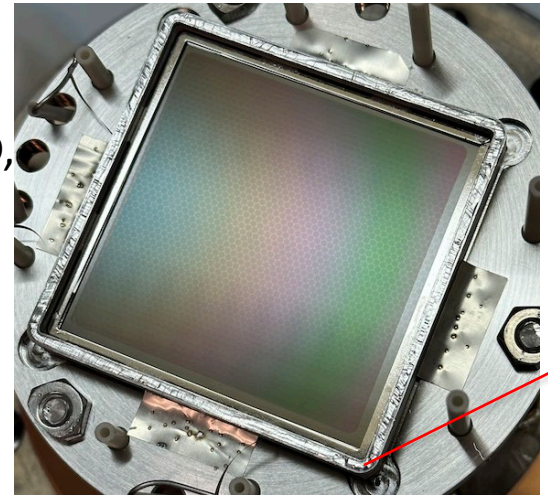


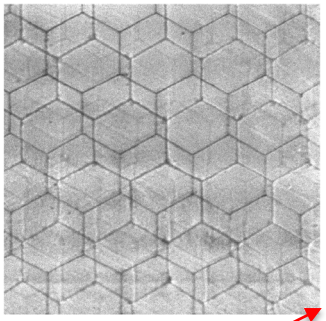


54 x 54mm Incom 10 µm pore, 13° bias, 70% OAR, L/D 60:1, MgO ALD chevron.



CsI 54mm ALD, MCP 10µm Planacon

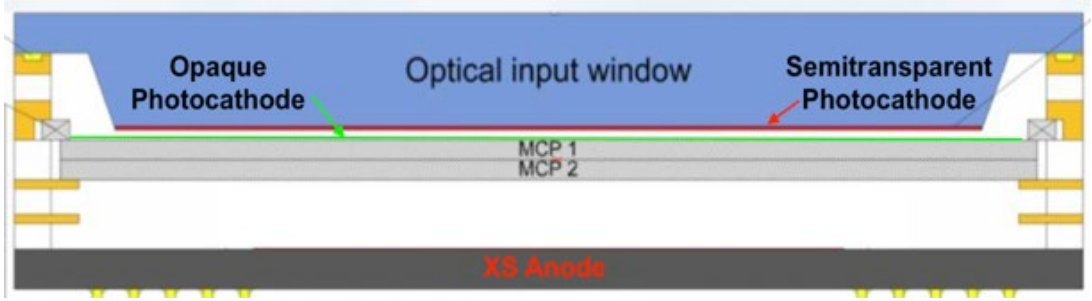




Similar behavior and performance

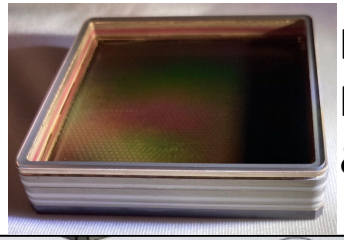
10cm, 10µm, ALD MCP Background
0.060 cts / sec / cm^2

Cross Strip Readouts in Planacon Sealed Tubes

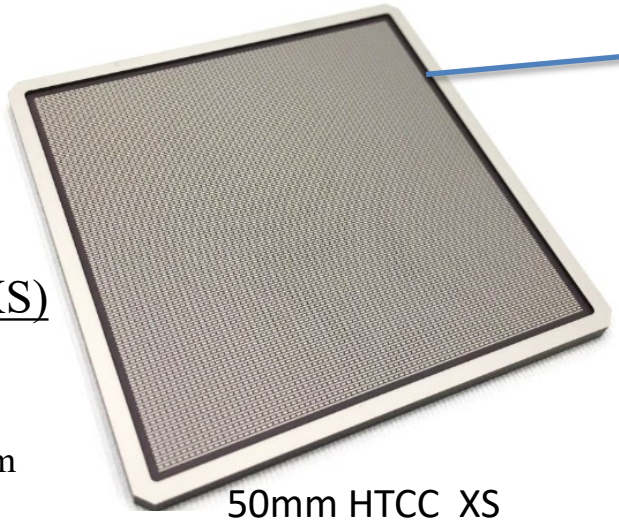


Cross section of a 100mm XS tube. UV input window can be coated with a bialkali cathode, or an opaque cathode can be used on the top MCP. A pair of 10 µm ALD MCPs provides signal amplification and an XS anode is the readout.

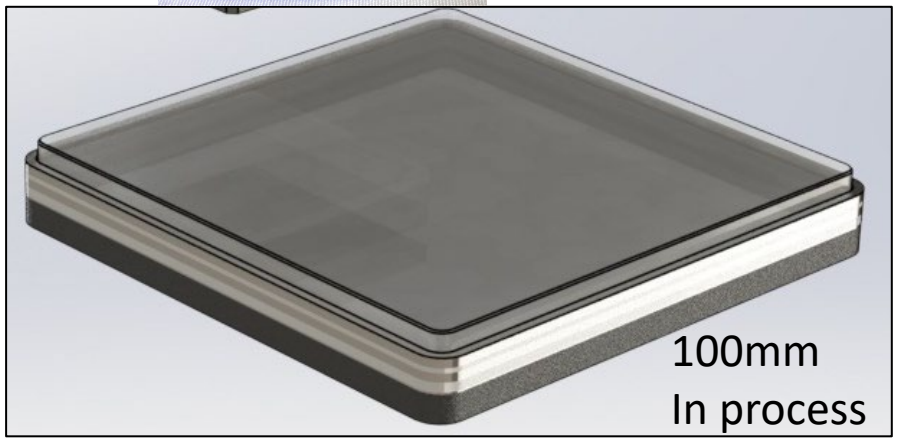
We have designed and are fabricating a 100mm format device with a UV window, a pair of 10 µm ALD MCPs and an XS anode readout. The techniques follow those used for the recent 50mm XS Planacon tubes.



Existing 50mm Planacon XS tube(s) & elevated to TRL 5/6



50mm HTCC XS (High temperature co-fired ceramic).

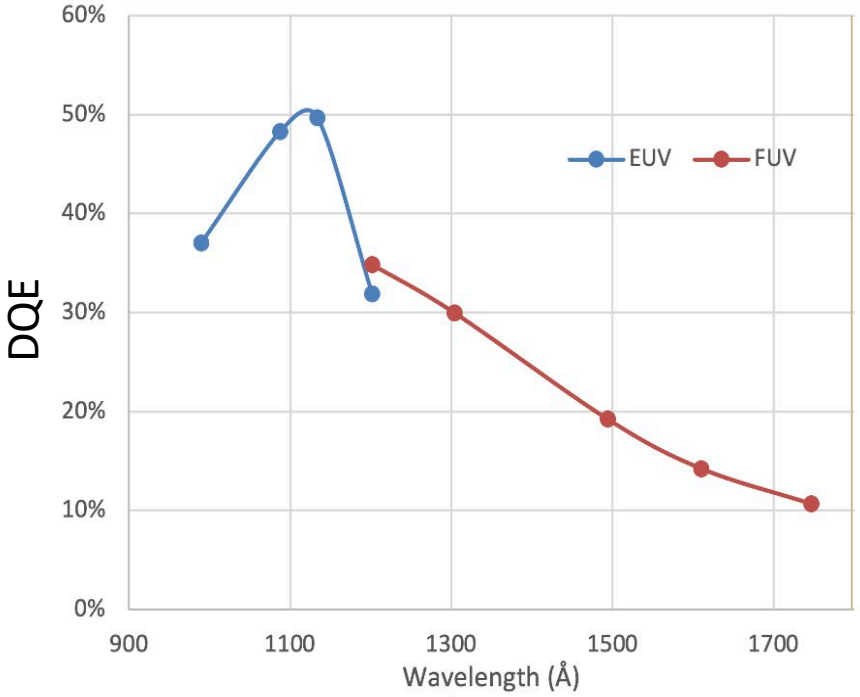


100mm
In process

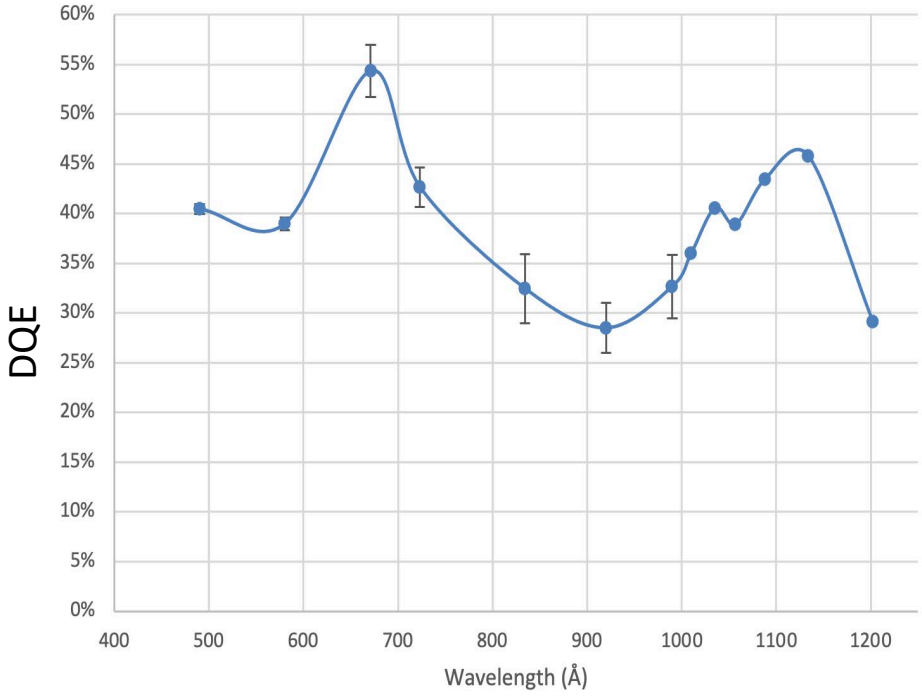
Cross- Strip (XS)

- Gain ~10^6
- Rate <5MHz
- Size ~1cm to 20cm
- Spatial resolution:
  - ~15µm <5cm
  - <= 25µm ≥10cm

Opaque Photocathodes On ALD MCPs
Latest MCPs Demonstrate High DQE – Eg: CsI.
(bialkali & GaN for >120nm – 350nm,
KBr, KI, etc for 5nm – 100nm)



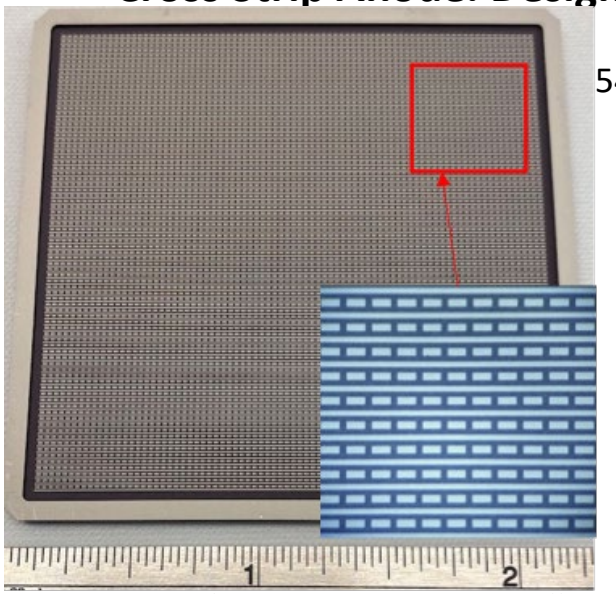
Recent CsI results (May 23) using 10 µm pore MCP material show good QE results.



Recent results (Oct 23) using a different batch of 10 µm pore MCP material also show very good QE results.

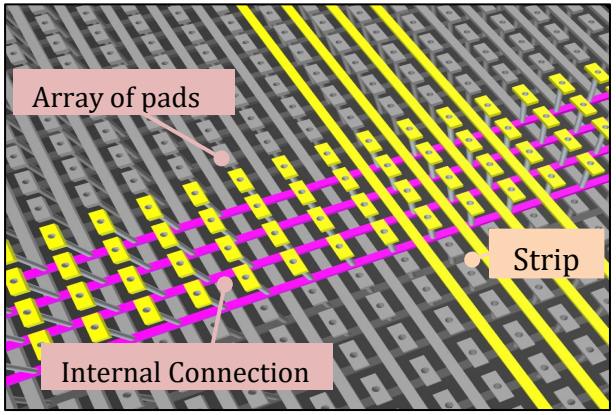
Cross Strip Anodes – HTCC (Ceramic)

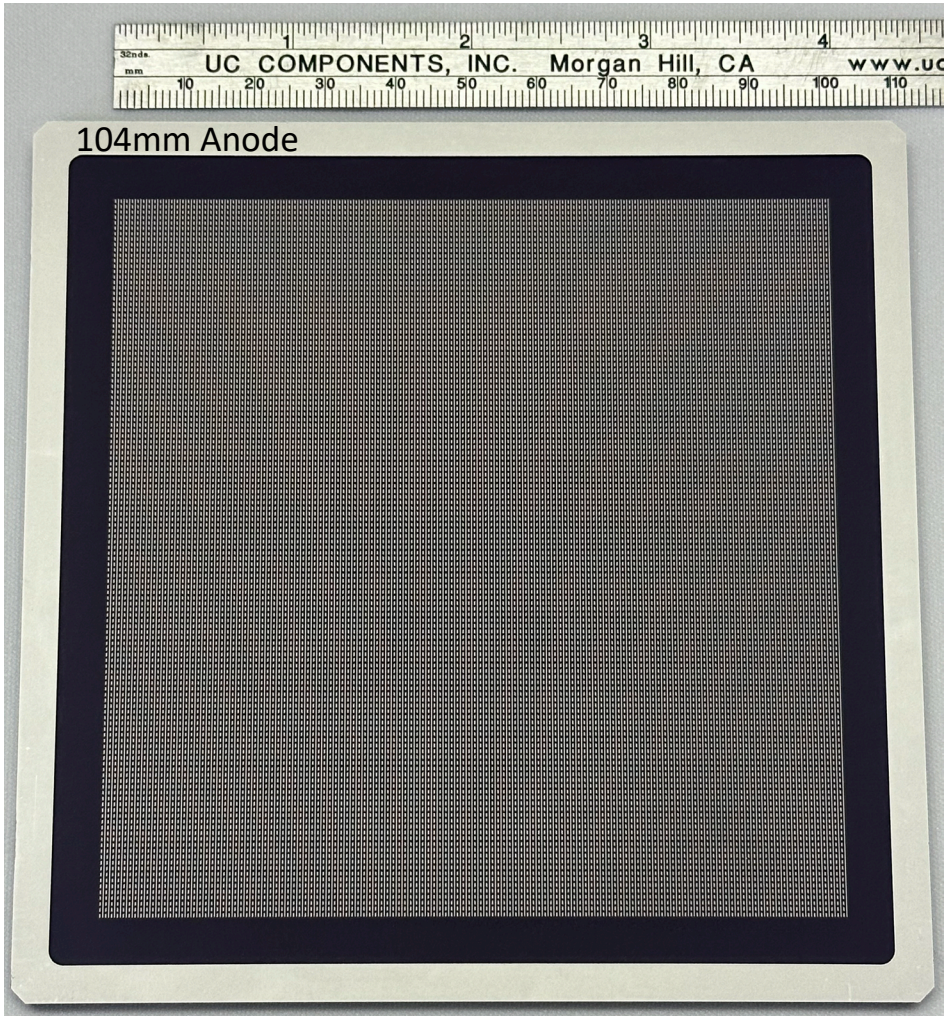
High Temperature Cofired Ceramic (HTCC), 54mm & 104 mm square Cross Strip Anode. Designed in collaboration with Kyocera.



54mm anode

Anode active area has no open vias at all in this design using robust HTCC methodology. Design eliminates through holes and minimizes parasitic capacitance. Economical piece part cost even with tooling/setup costs. Long delivery, **just arrived,** 100mm XS anodes.

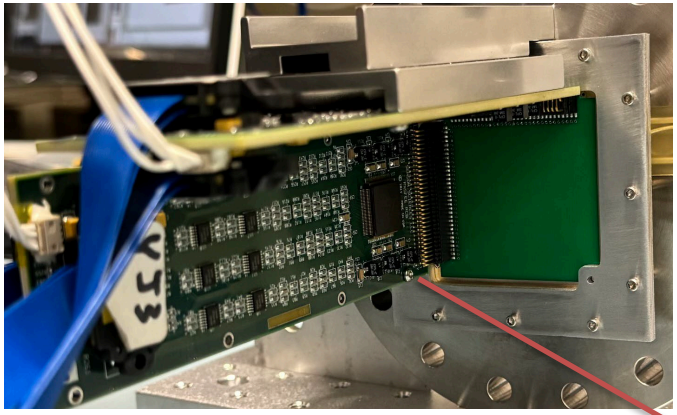




104mm Anodes currently in bench test, then will be used with MCPs in an open face detector for operational validation before making sealed tube(s).

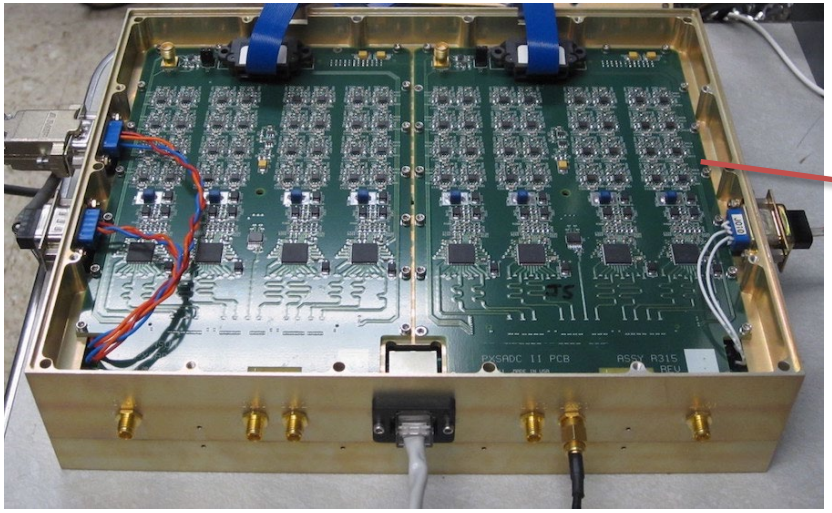
GRAPH - ASIC Electronics for XS Event Encoding

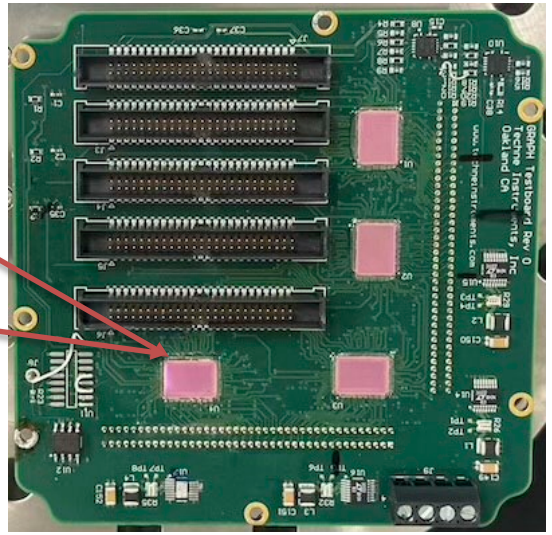
PXSII SMT amplifier



Earlier PXSII electronics has separate preamplifier boards and ADC/FPGA boards. Flown successfully on CHESS, INFUSE, 5x, but is bulky and heavy and draws 25w for a 50mm detector. We are implementing an ASIC version of the Cross Strip processing electronics – GRAPH. This implements charge sensitive amplifier (CSA) and fast ADC into single device, 46mW/channel, ~7.4W = (2.4W + FPGA power draw) for 50mm XS, ~15W for 100mm XS. This has been prototyped and is being functionally tested and about to be used to process XY photon events on a 50mm XS detector.

PXSII SMT Digitizer and FPGA

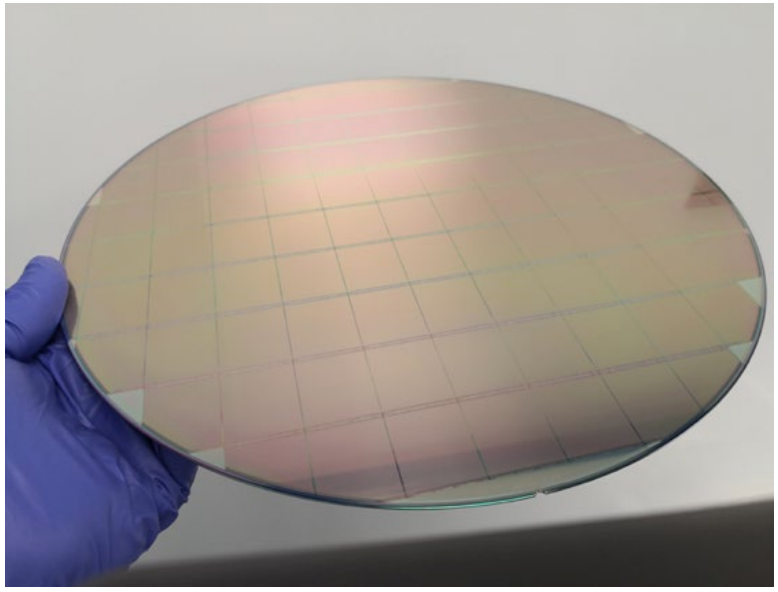




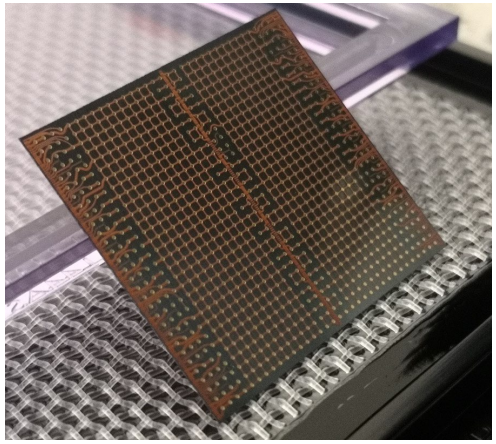
4x GRAPH test board, 16 channels per ASIC

Timepix 4 – Mosaicing a pixelized MCP readout

- 512 x 448 pixelated readout ASIC (28x25mm) **Factor of 4 larger than Tpx3**
- **Large area tiling** using "Through Silicon Via" technology to bring signals to back of die (4-side abuttable)
- Amplifier/ADC in each 55µm pixel
- Hit pixels measures both input amplitude and time of arrival
- 75e- RMS noise for charge measurement
  - SNR > 100 allowing sub-pixel centroid accuracy
- Data-driven readout (shutterless)
- 2 Gigahits per second maximum output
- Designed by CERN Microelectronics Group



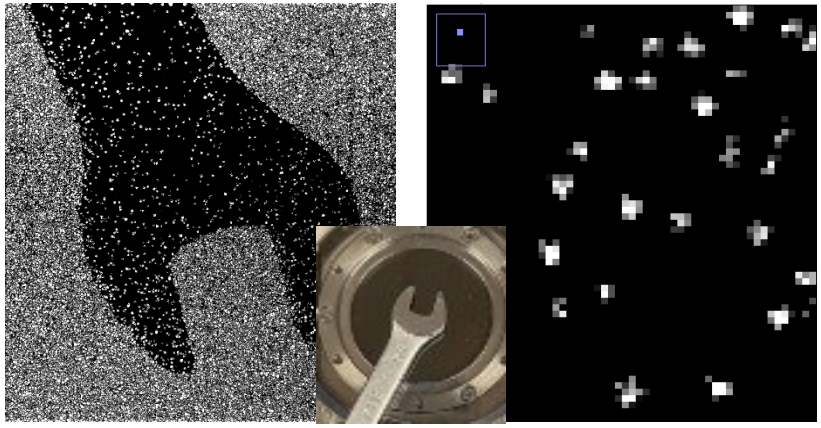
30cm TSMC CMOS wafer of Tpx4 dies



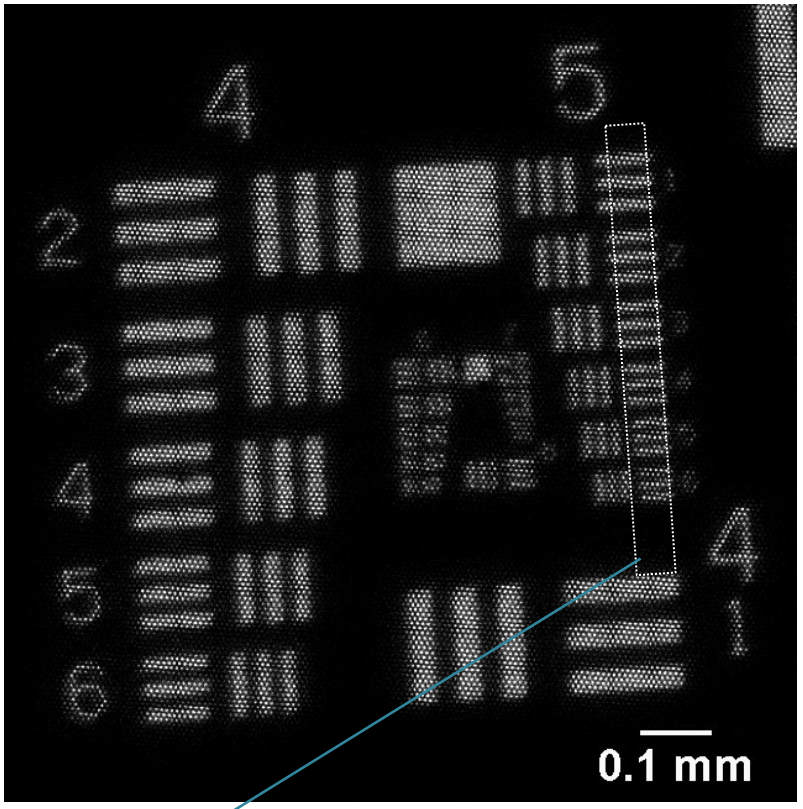
Backside BGA pattern – no wirebonds!

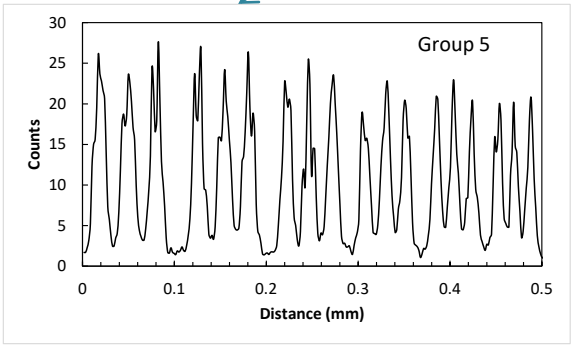
Timepix 4 – Advantages

- Extremely high resolution at low gain (lower HV and longer lifetime of MCP)
- Maintains performance when scaled to large area
- Huge dynamic range – Global 20 MHz event rate with centroiding
- Local pixel rate limit ~ 10 kHz, consistent with MCPs
- Data driven readout (photon counting)



First light - Tpx4 readout of MCP





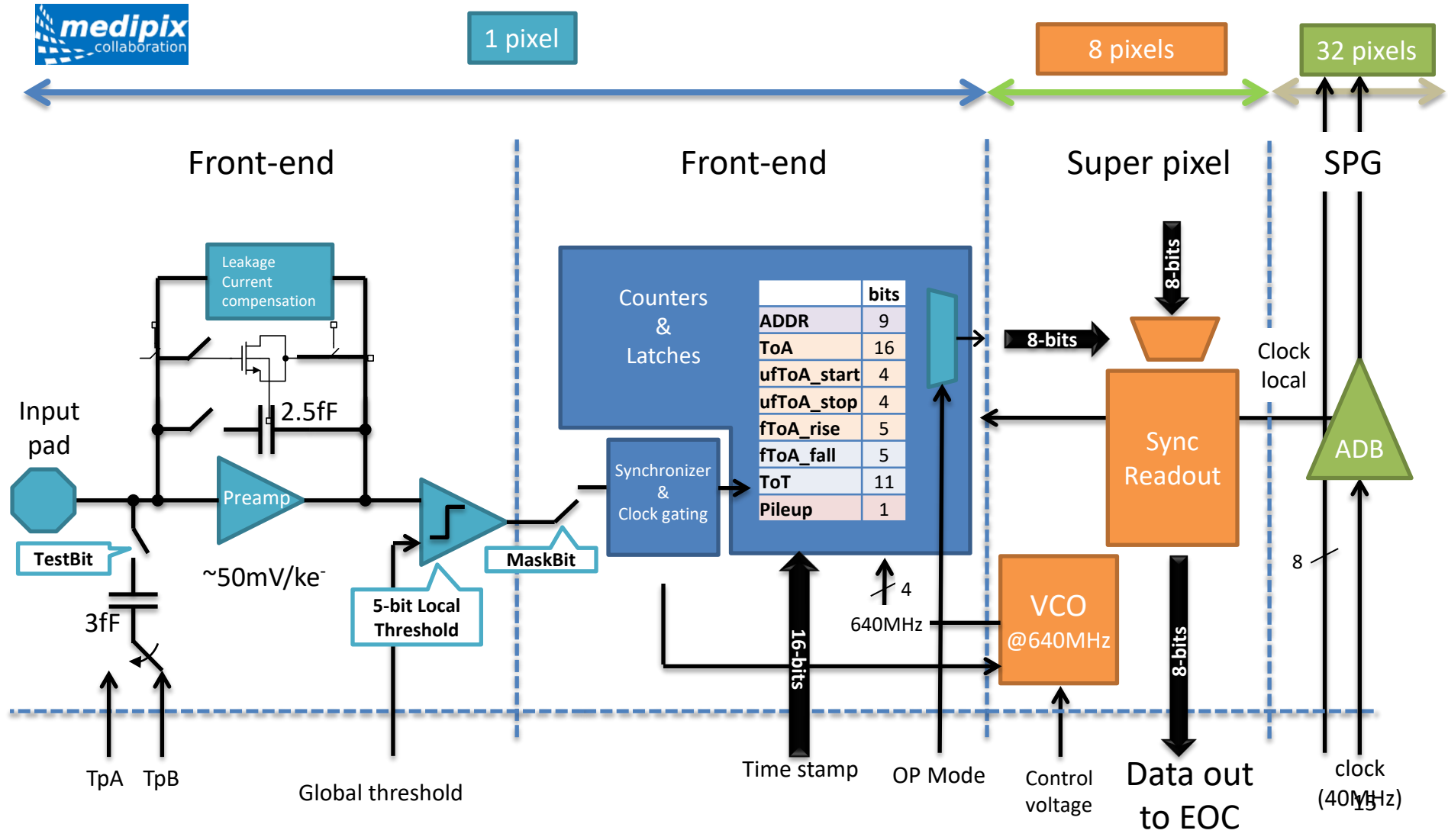
USAF test pattern showing resolution better than 64lp/mm using Timepix readout

MCP detector developments for the next generation of space missions:

200mm 10μm MCP formats	Up to 200mm demonstrated
Curved focal planes	Cylindrical demonstrated
High QE 100nm – 350nm	>50% CsI demonstrated, Bialkali 30% @ 180nm, 360nm cutoff
Low Flat field modulation	ALD MCPs ≤20% hex pattern ~1 resel wide
Improved MCP gain stability	>5 x 10^{13} events cm^{-2} demonstrated
Low background rates ---	<0.06 $cm^{-2}s^{-1}$ demonstrated up to 20cm
Low radiation sensitivity	Achieve 0.7 % MeV gamma efficiency
Large XS readout formats	100mm demonstrated, 200mm possible
Open face and sealed tubes	Up to 100mm open face, 50mm Planacon XS demonstrated, 100mm sealed tubes in progress.
Spatial resolution ≤25μm FWHM	100mm format demonstrated
High performance electronics with low power/volume /mass	GRAPH ASIC in development for XS anodes Tpx4 ROIC as scalable high performance anode

Backup Slides

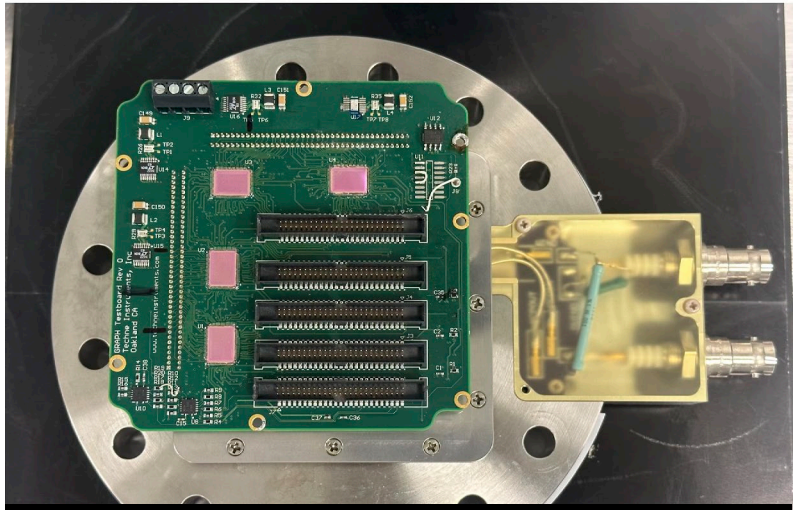
Timepix4 Single Pixel Schematic (1 of 230k)



Testing of the GRAPH ASIC for Processing Photon Event Positions on Cross Strip Anodes

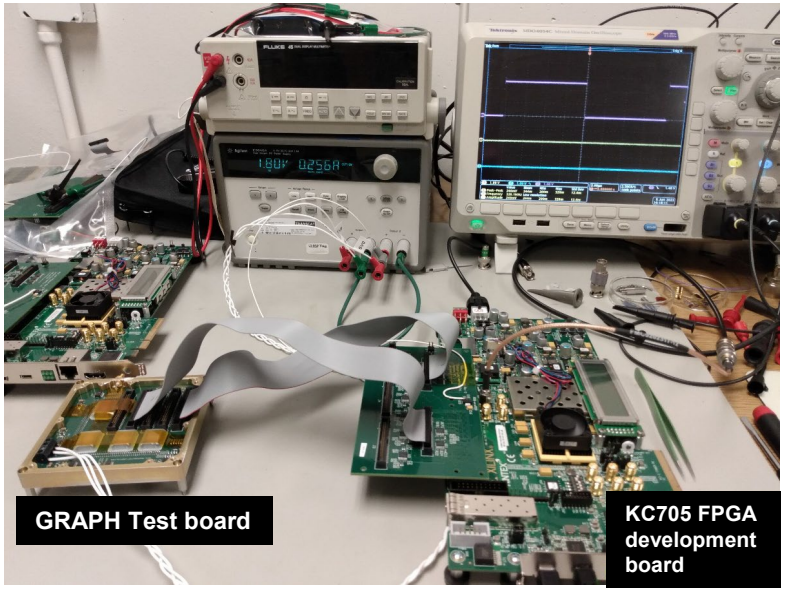
#2365

- Firmware has been commissioned for multi-ASIC readout & high-speed Ethernet data interface.
- Python-based S/W for scriptable testing and large dataset aggregation is also implemented.

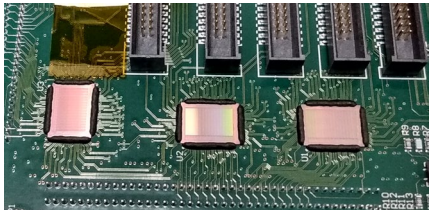


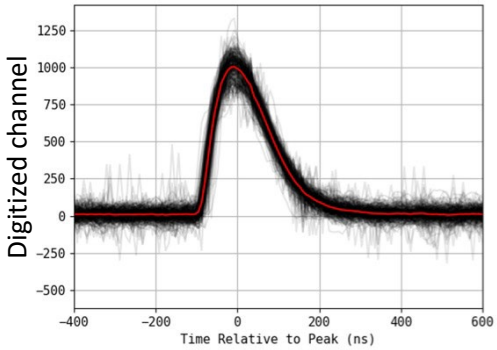
GRAPH Test board mounted to the 50mm XS anode of a sealed tube Planacon detector.

Initial test functionality and FW/SW development setup.



- First generation ASICS are wire bonded directly to test boards to give a 32 channel X and 32 channel Y capability
- Test boards can be mounted directly to anode / detector backplane, and then to an FPGA board behind that.

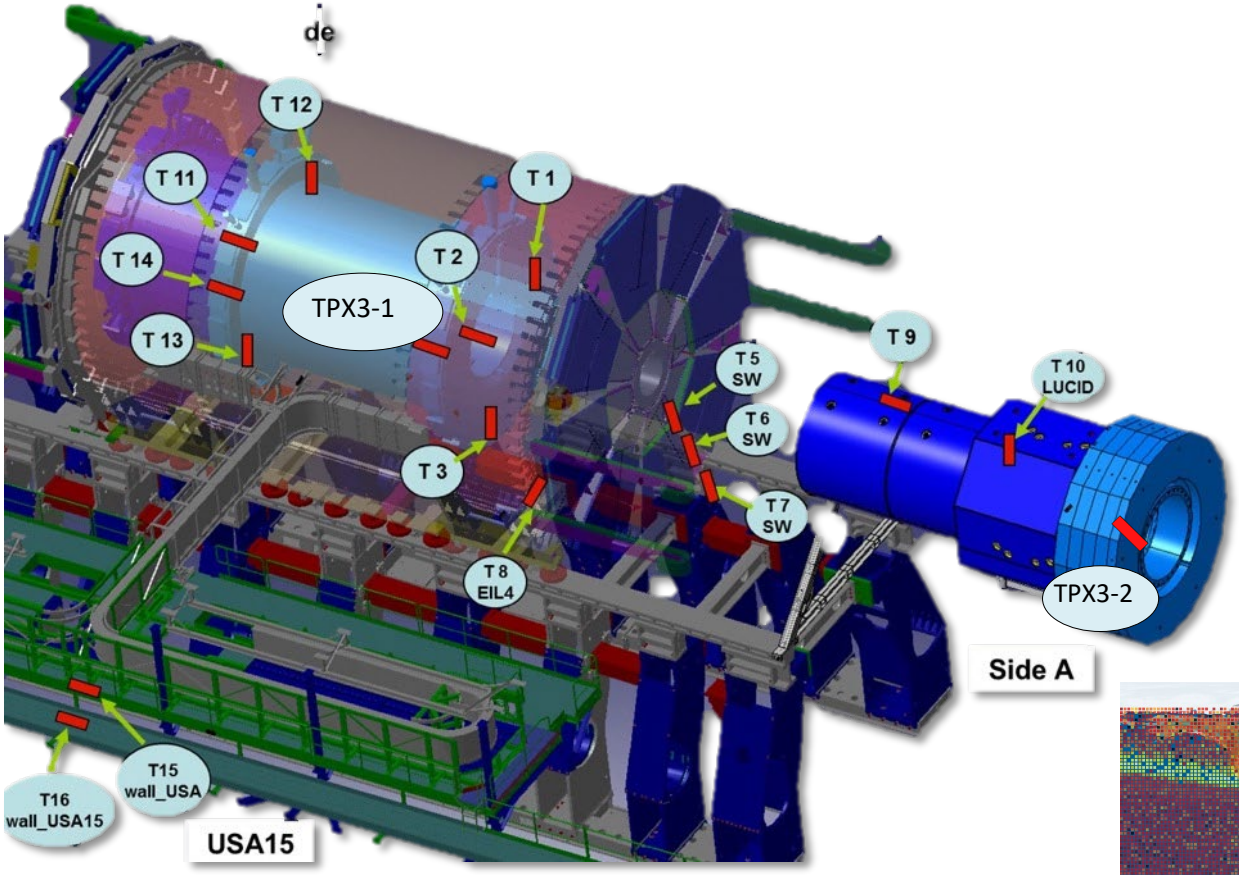


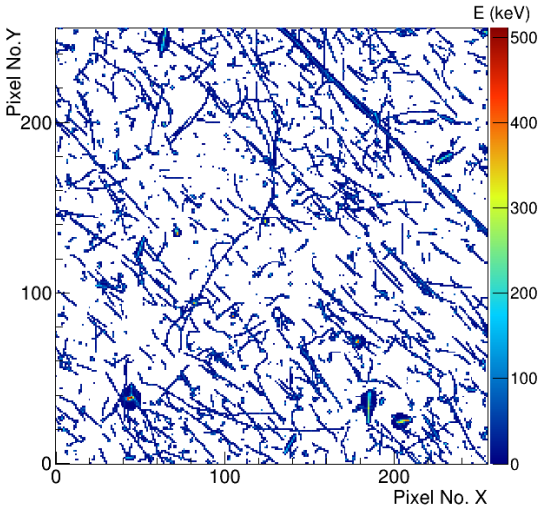


Charge injection input: ~50fC pulse. Output: ~250 trace captures, average trace overlaid (red) equates to ~1000 ADC counts, ~300e-/ADC count. Typical peak for MCP signals @~ 2 x 10^6 gain spread over 5-7 XS strips.

Custom ASIC implements charge sensitive amplifier (CSA) and fast ADC into single 16 channel device, 11 x 9 mm size. 46mW/channel, ~7.4W = (2.4W + FPGA power draw) for 50mm XS Planacon, ~15W for 100mm XS. 160ns CSA return to baseline allows high counting rates (~10% deadtime at 6MHz). Multi-photon recognition and processing algorithms should increase this substantially.

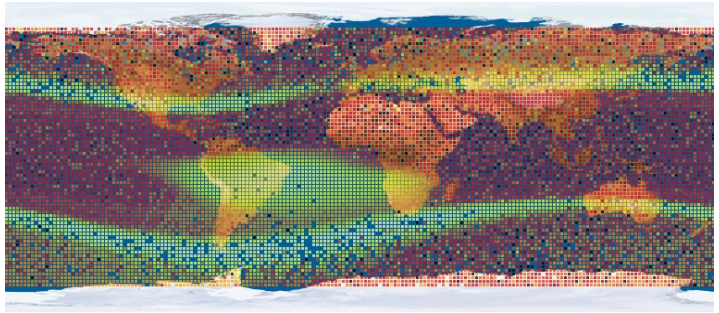
Radiation tolerance





Location of Timepix detectors in LHC - ATLAS

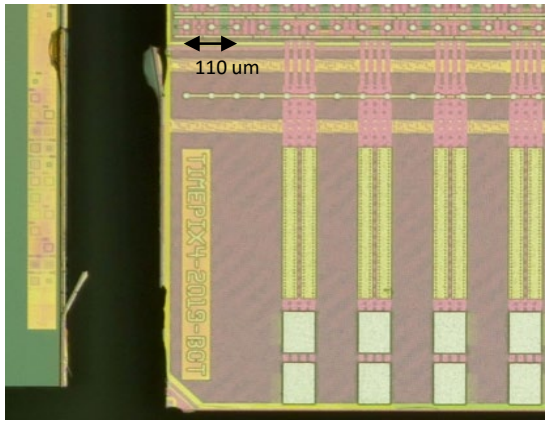
B. Bergmann *et al.,* "Relative luminosity measurement with Timepix3 in ATLAS", *JINST* **15** C01039, 2020.



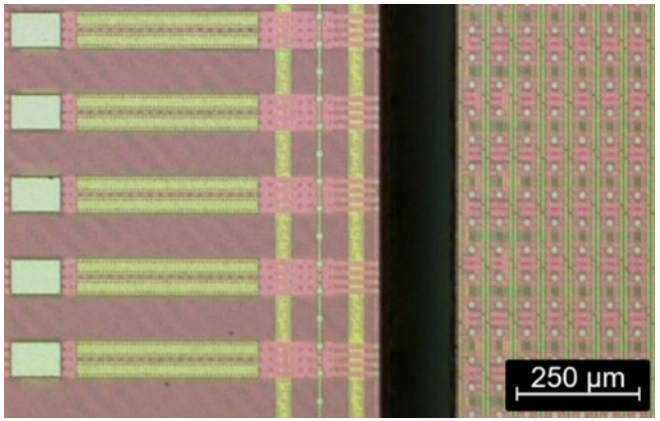
Dose distribution in orbit measured with SATRAM. From: https://satram.utef.cvut.cz

Stealth Dicing tests

- To minimize gaps between ASICs and therefore better event centroids at these interfaces, the ASIC dicing from the wafer must be very accurate and reproducible.
- Stealth Laser dicing uses a focused laser beam to modify the Si crystal structure, making it weaker, so when the wafer is stretched, it naturally cleaves at these laser defined boundaries. Front side laser ablation is used first in order to reduce meandering related to metal layers separation.
- Experiments with actual Tpx4 wafer fragments showed clean, debris free edges estimated to be rough at 10 microns, sufficient for 55µm spacing between ASIC dies.



#1. First test of Si Stealth dicing. Very accurate silicon cleaving but top metal surface shows "meandering" and therefore must be removed first with laser ablation.



#2. Second test of Si Stealth dicing, this time with laser ablation of metal layers. Test was a success!. Clean cuts estimated to be rough to 10 microns, a small fraction of a 55µm pixel (seen on right)